

IN THE CLAIMS

1. (*Currently Amended*) A power semiconductor device having high avalanche capability, said device comprising:

a semiconductor substrate with two ~~sides~~ surfaces, and an N+ doped layer extending into the substrate from one surface ~~of the device into the~~
5 ~~substrate~~ thereof, an N- doped layer over the N+ doped layer, a P- doped well formed in the N- doped layer and extending from the other surface of the ~~device~~
substrate into the N- doped layer, a P+ doped region formed in the P- doped well and ~~also~~ extending from the other surface of the ~~device~~ substrate into the
P-doped well, the P- doped well defining an upwardly curving junction between
10 the P- doped well and the N- doped layer, said upwardly curving junction extending from the lower end of the P- doped well to the other surface of the
~~device~~ substrate, and an N+ doped region formed in the other surface of the
~~device~~ substrate and in the N- doped layer, said N+ region laterally spaced from
the P+ doped region and the P-doped well, said P- doped well and P+ doped
15 region having a combined thickness of about 5 μ m to about 12 μ m; and
recombination centers comprising noble metal impurities disposed
substantially in said N - doped layer and P - doped well.

2. (*Currently Amended*) The device of claim 1 wherein said P - doped well has a thickness of about 4 ~~[[pm]]~~ μm to about 10 μm .
3. (*Currently Amended*) The device of claim 1 wherein said P+ doped region has a thickness of about 0.1 ~~[[gm]]~~ μm to about 2 μm .
4. (*Previously Presented*) The device of claim 1 wherein said P - doped well has a dopant level of at least 10^{16} atoms/cm³.
5. (*Previously Presented*) The device of claim 4 wherein said P - doped well has a dopant level of about 2.5×10^{17} atoms/cm³.
6. (*Previously Presented*) The device of claim 1 wherein said P+ doped region has a dopant level of at least 10^{18} atoms/cm³.
7. (*Previously Presented*) The device of claim 6 wherein said P+ doped region has a dopant level of about 6×10^{19} atoms/cm³.
8. (*Currently Amended*) The device of claim 1 wherein said N - doped layer has a dopant level of about 10^{14} atoms/cm³ to about 10^{15} ~~atoms/cm³~~ atoms/cm³.

9. *(Cancelled)*.
10. *(Original)* The device of claim 1 wherein said noble metal impurities are selected from the group consisting of gold, platinum, and palladium.
11. *(Original)* The device of claim 10 wherein said noble metal impurities comprise platinum.
12. *(Previously Presented)* The device of claim 11 wherein said recombination centers are formed by platinum diffusion through said N + doped substrate into said N - doped and P - doped well.
13. *(Original)* The device of claim 11 containing platinum impurities at a concentration of about 1×10^{15} to about 1×10^{16} atoms/cm³.
14. *(Original)* The device of claim 13 wherein said concentration of platinum impurities is about 2×10^{15} atoms/cm³.
15. *(Original)* The device of claim 1 further comprising an N + doped region disposed in said N - doped layer.
16. *(Cancelled)*.

17. (*Previously Presented*) The device of claim 16 comprising a diode,
MOSFET or an IGBT power device.